Digital Electronics

Final Examination

Part A

Spring 2009

PRACTICE EXAM

Student Name: _____

Date: _____

Class Period: _____

Total Points: _____ /40

Converted Score: _____ / 50

Multiple Choice

Directions: **Select the letter of the response which best completes the item or answers the question.**

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1. If an integrated circuit has been damaged and you smell smoke, you should_____.

A. leave the power on while pulling out the damaged integrated circuit.

B. turn the power off for a few minutes before pulling out the damaged integrated circuit.

C. push down on all the integrated circuits in the circuit with your finger.

D. turn up the power to twice the voltage before pulling out the damaged integrated circuit.

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2. In scientific notation, which prefixes are used for values smaller than a whole value?

A. Kilo, milli, micro

B. Mega, micro, nano

C. Nano, micro, mega

D. Micro, nano, milli

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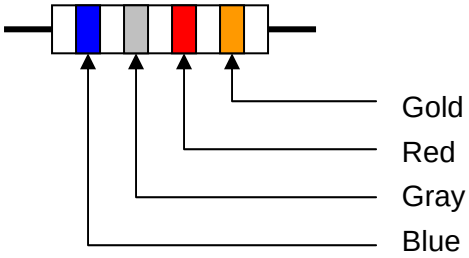
3. What is the value of the resistor shown below?



A. 6.8 K Ω ±10 %

B. 28 M Ω ±5 %

C. 6.8 K Ω ±5 %

D. 180 Ω ±10 %

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4. What are the color bands for a 390 Ω (±10) resistor?

A. RED-BLUE-BLACK-GOLD

B. GREEN-BLUE-RED-SILVER

C. RED-GREEN-BLACK-SILVER

D. ORANGE-WHITE-BROWN-SILVER

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5. In a parallel circuit, you measure 1.5 mAmps flowing through a 600 Ω resistor. What is the voltage drop across the resistor?

A. 2.5 μ Volts
B. 900 m Volts
C. 400 m Volts
D. 0.900 m Volts

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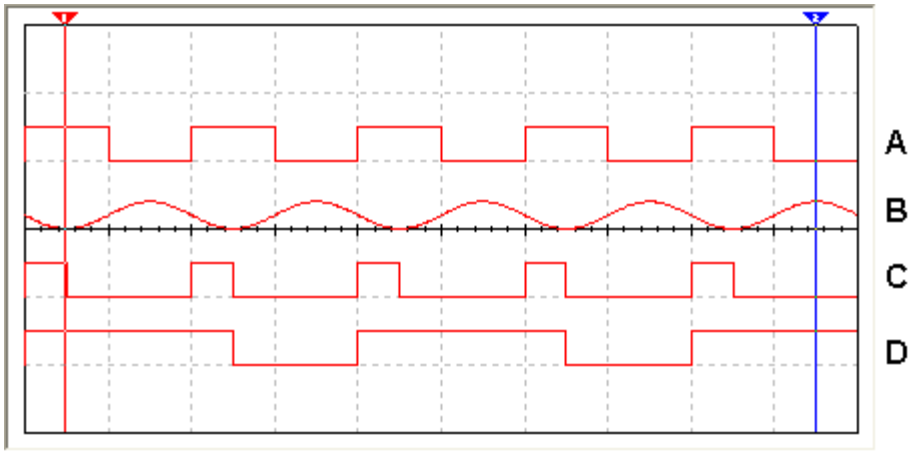
6. Which of the waveforms shown below is <u>not</u> a digital waveform?



A. Waveform A
B. Waveform B
C. Waveform C
D. Waveform D

---

7. What is the decimal equivalent to the binary number 010110_2?

A. 22_{10}
B. 13_{10}
C. 23_{10}
D. 42_{10}

---

8. In the eight-bit binary number shown below, which bit is the Least Significant Bit (LSB)?

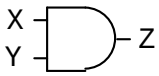
B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
1	0	1	1	0	1	0	1

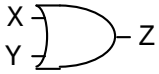
A. B_7
B. B_0
C. B_7 - B_4
D. B_3 - B_0

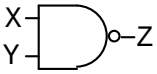
---

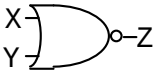
9. The truth-table shown below represents which of the following gates?

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

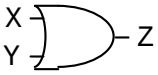
A. 

B. 

C. 

D. 

10. The gate shown below is represented by which of the following truth-tables?



A.

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

B.

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

C.

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

D.

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

11. Which of the following is a rule of Boolean algebra?

A. $A \bullet 0 = A$

B. $A \bullet 1 = 1$

C. $A \bullet A = A$

D. $A \bullet \overline{A} = 1$

12. Which of the following is an example of the Associative Law of Boolean algebra?

A. $X + (Y + Z) = (X + Y) + Z$ ***C.*** $X + Y = Y + X$

B. $X(Y + Z) = XY + XZ$ ***D.*** (W + X)(Y + Z) = WY + WZ + XY + XZ

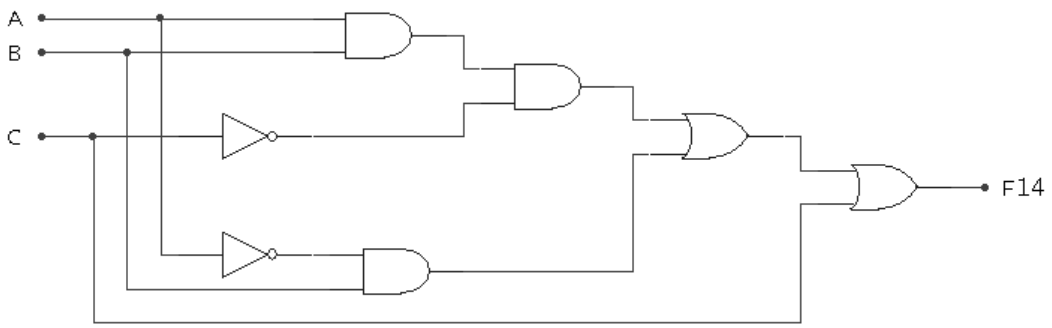
13. Which of the following equations is the *un-simplified* Sum-Of-Products equation for the truth table shown?

A	B	C	F_{13}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

A. $F_{13} = \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C} + A\,B\,C$ ***C.*** $F_{13} = (A + \overline{B} + C)(\overline{A} + B + C)(\overline{A} + \overline{B} + C)(\overline{A} + \overline{B} + \overline{C})$

B. $F_{13} = A\,\overline{B}\,C + \overline{A}\,B\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C}$ ***D.*** $F_{13} = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}\,C$

14. Which of the following un-simplified Boolean expressions represents the logic circuit shown below?



A. $F_{14} = A\,\overline{B} + A\,\overline{B}\,C + C$ ***C.*** $F_{14} = A\,\overline{B}\,\overline{C} + \overline{A}\,B + C$

B. $F_{14} = A\,B\,\overline{C} + \overline{A}\,B + C$ ***D.*** $F_{14} = A\,\overline{B} + \overline{A}\,B\,C + \overline{C}$

15. Which of the following is a correct DeMorgan's Identity?

A. $\overline{X + Y} = \overline{X} \bullet \overline{Y}$

B. $\overline{X + Y} = X + Y$

C. $\overline{X + Y} = X \bullet Y$

D. $\overline{X + Y} = \overline{X} + \overline{Y}$

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16. Which of the following K-Maps has the 1's & 0's properly placed for the function F_{16} ?

$$F_{16} = A\,\overline{B} + \overline{A}\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,D$$

A.

	$\overline{A}\,\overline{B}$	$\overline{A}\,B$	$A\,B$	$A\,\overline{B}$
$\overline{C}\,\overline{D}$	0	1	0	0
$\overline{C}\,D$	0	1	1	0
$C\,D$	0	1	0	0
$C\,\overline{D}$	0	1	1	1

B.

	$\overline{A}\,\overline{B}$	$\overline{A}\,B$	$A\,B$	$A\,\overline{B}$
$\overline{C}\,\overline{D}$	0	0	0	1
$\overline{C}\,D$	1	0	0	1
$C\,D$	0	0	0	1
$C\,\overline{D}$	1	1	0	1

C.

	$\overline{A}\,\overline{B}$	$\overline{A}\,B$	$A\,B$	$A\,\overline{B}$
$\overline{C}\,\overline{D}$	0	0	0	1
$\overline{C}\,D$	0	1	0	1
$C\,D$	0	0	0	1
$C\,\overline{D}$	1	1	0	1

D.

	$\overline{A}\,\overline{B}$	$\overline{A}\,B$	$A\,B$	$A\,\overline{B}$
$\overline{C}\,\overline{D}$	1	0	1	0
$\overline{C}\,D$	1	0	0	0
$C\,D$	0	0	0	0
$C\,\overline{D}$	1	1	1	1

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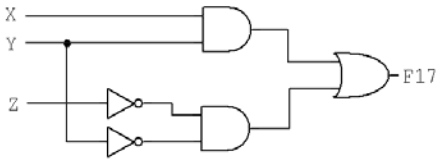
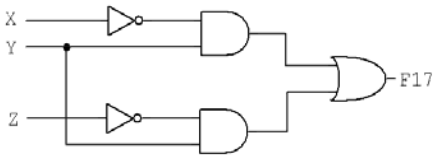
17. Which of the following logic circuits correctly implements the Boolean equation :

$$F_{17} = X\,\overline{Y} + Y\,\overline{Z}$$

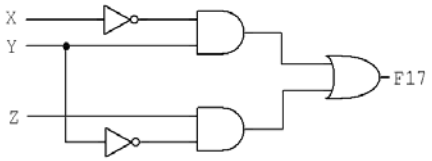
A.



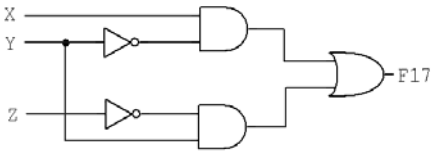
B.



C.



D.



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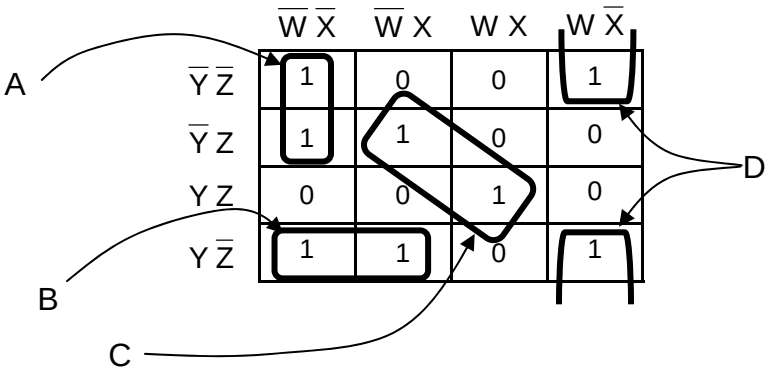
18. How many different input conditions will produce a HIGH output on a three-input OR gate?

A. 3
B. 5
C. 8
D. 7

19. Which of the following k-map groupings is not legal?



A. *Group A*
B. *Group B*
C. *Group C*
D. *Group D*

20. Which of the following Boolean equations is in Product-Of-Sums form?

A. $F_{20} = (\overline{A} + B + \overline{C})(\overline{A} + C)(A + \overline{B} + C)$
B. $F_{20} = \overline{A}\,B\,C + A\,(\overline{B} + C)$
C. $F_{20} = \overline{A}\,(B + C) + A\,(\overline{B} + C)$
D. $F_{20} = A\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{C}$

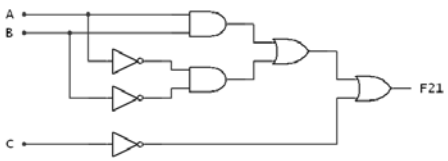
21. The three circuits shown below all implement the logic equation:

$$F_{21} = A\,B + \overline{A}\,\overline{B} + \overline{C}$$

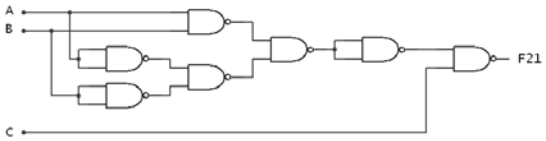
Of these circuits, which one would require the least number of IC chips?

A. They all require the same number of IC chips.

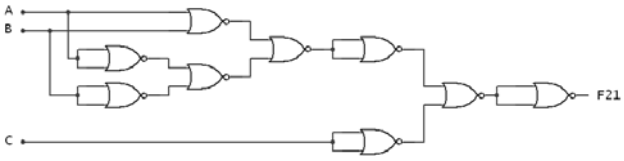
B.



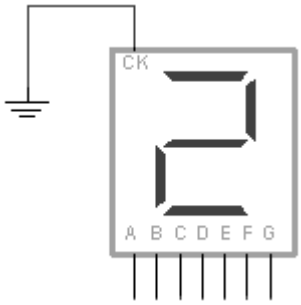
C.



D.



22. What logic values need to be placed on the inputs (a) through (g) of the common-cathode seven segment in order to display the number 2?



A.

A	B	C	D	E	F	G
1	1	0	1	1	0	1

B.

A	B	C	D	E	F	G
0	0	1	0	0	1	0

C.

A	B	C	D	E	F	G
1	0	1	1	0	1	1

D.

A	B	C	D	E	F	G
0	1	1	0	0	1	0

23. When typing the Boolean expression $A = X + \overline{Y}\,Z$ into the WinCupl program, which of the following expressions would be entered?

A. $A = X + \overline{Y}\,Z$

B. $A = X * Y' + Z$

C. $A = X \ \#\ !Y \ \&\ Z$

D. $A = X$ OR NOT(Y) AND Z

24. When comparing a PLD circuit to a logic circuit implemented with individual logic gates, the PLD circuit will _____.

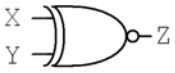
A. be easier to breadboard with fewer chips and wires.

B. require you to simplify the expression using a K-Map.

C. require more chips and wiring.

D. require a higher operating voltage.

25. The gate shown below is represented by which of the following truth-tables?



A.

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

B.

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

C.

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

D.

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

26. Which of the following is the correct truth-table for a half-adder?

A.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

B.

A	B	Sum	Carry
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

C.

A	B	Sum	Carry
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

D.

A	B	Sum	Carry
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	1

27. How are the Q and $\overline{Q}$ outputs of a flip flop affected by setting the active low *asynchronous* RESET input to a logic zero?

A. $Q = 1$ and $\overline{Q} = 0$

B. $Q = 0$ and $\overline{Q} = 1$

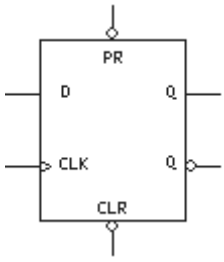
C. $Q = 1$ and $\overline{Q} = 1$

D. No change.

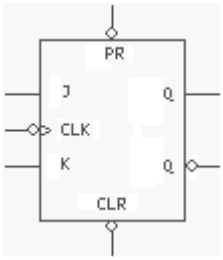
---

28. Which of the devices is a Negative Edge Triggered J-K flip-flop?

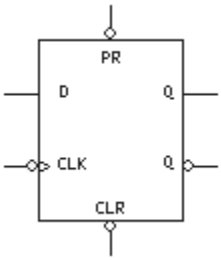
A.



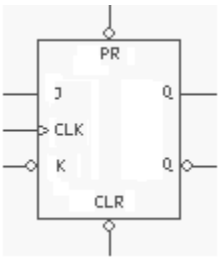
B.



C.



D.



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29. How many flip-flops are required to implement a divide-by-4 circuit?

A. 4

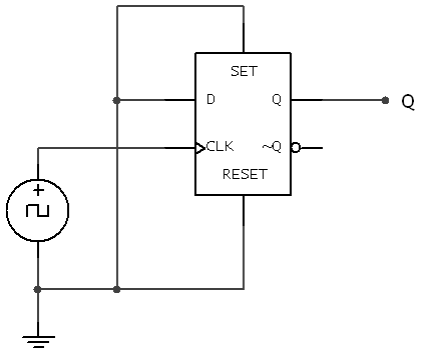
B. 3

C. 2

D. 1

---

30. For the single flip-flop shown below, what will the output Q be on the next clock pulse?



A. Q will be high.

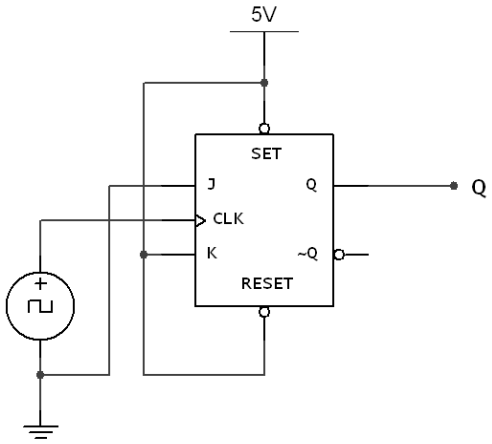
B. Q will be low.

C. Q will toggle.

D. Q will not change.

---

31. For the single flip-flop shown below, what will the output Q be on the next clock pulse?



A. Q will be high.

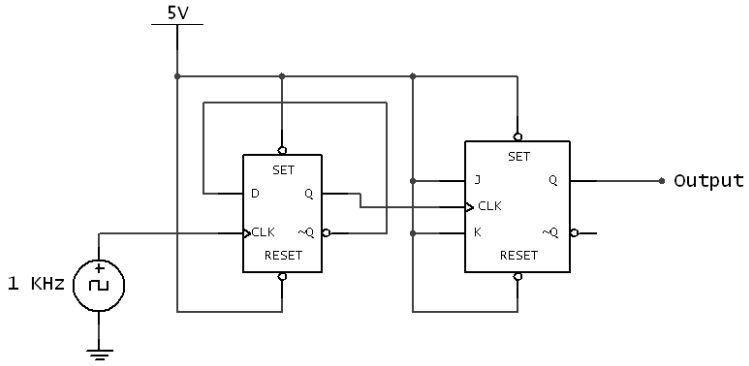
B. Q will be low.

C. Q will toggle.

D. Q will not change.

---

32. Determine the output frequency for the circuit shown below.



A. 2 KHz.

B. 500 Hz.

C. 1 KHz.

D. 250 Hz.

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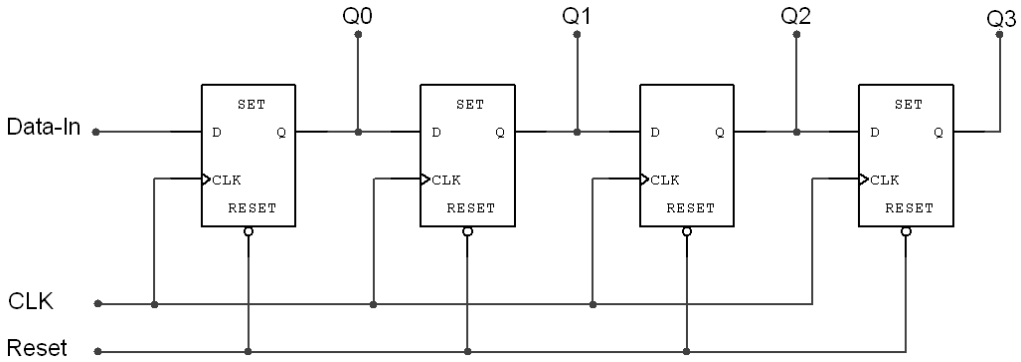
33. The shift register shown below is what type?



A. Serial-In / Serial-Out

B. Serial-In / Parallel-Out

C. Parallel-In / Parallel-Out

D. Parallel-In / Serial-Out

---

34. Which of the following statements applies to asynchronous counters?

A. Asynchronous counters are faster than synchronous counters.

B. Asynchronous counters require more power than synchronous counters.

C. All the flip-flops in an Asynchronous counter are clocked at the same time by a common external clock.

D. Asynchronous counters are also called ripple counters.

---

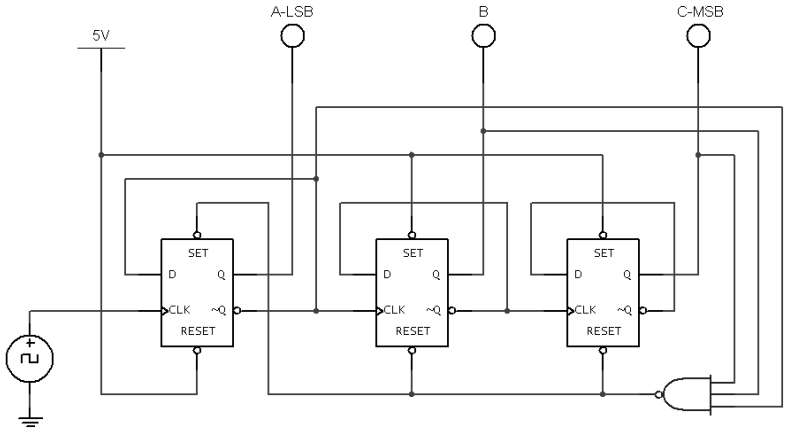
35. What is the minimum number of flip flops needed to build a mod 12 synchronous counter?

A. 2
B. 3
C. 4
D. 5

36. When you compare a counter design with discrete logic gates and flip-flops with an integrated counter, the integrated counter has the advantage of _____.

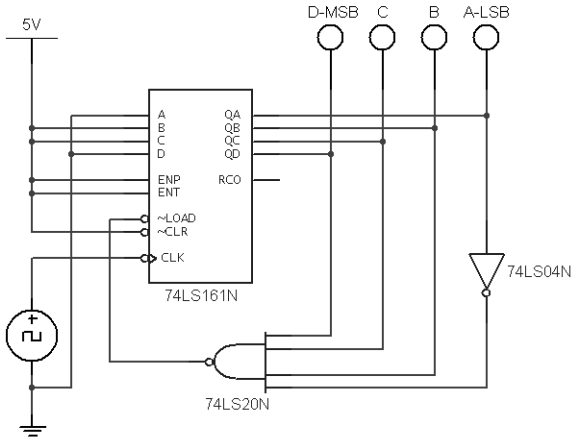
A. requiring fewer IC's.
B. requiring fewer wires.
C. requiring fewer parts.
D. All of the above.

37. What is the count range of the 3-bit asynchronous shown below?



A. 1 to 5
B. 1 to 6
C. 6 down to 1
D. 5 down to 1

38. What is the count range of the 4-bit synchronous shown below?



A. 14 to 6

B. 6 to 15

C. 6 to 14

D. 0 to 15

---

39. When you compare TTL logic gates to CMOS gates, the TTL gates have an advantage of having _____.

A. lower power consumption.

B. higher propagation delay.

C. higher noise margins.

D. less sensitivity to static electricity.

---

40. Noise Margin is _____.

A. a measure of the ability of a logic gate to drive further logic gates.

B. the time required for a signal to travel from the input of a logic gate to the output.

C. the difference between what a logic gate outputs as a valid logic voltage and what the input of the next gates expects to see as a valid logic voltage.

D. the difference in chip temperature from when the power is off to when the power is on.
