Digital Electronics™
Final Examination

Part C
College Credit Performance

Spring 2007

Student Name: _____

Date: _____

Class Period: _____

Total Points: _____/50

Design Problem

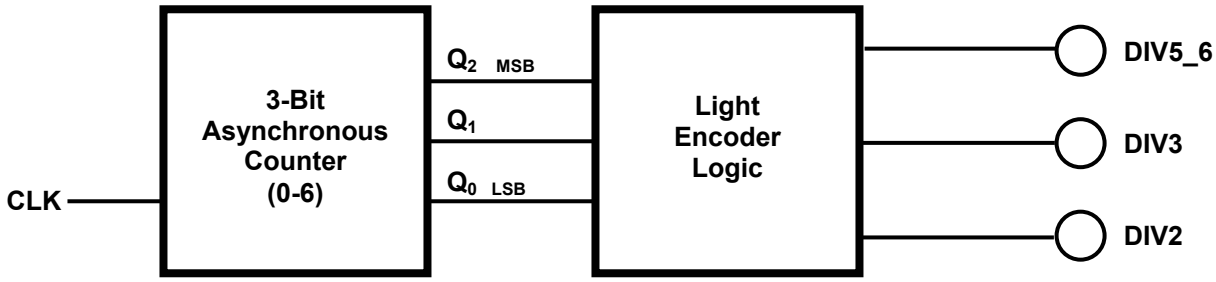
50 Points – Show ALL Work – Partial Credit May Be Awarded.

The ***Divisible Detector***, shown below, is a digital logic circuit that continuously counts from 0 (000) to 6 (110) and has three outputs that indicate if the count is divisible by (i) 5 or 6, (ii) 3 or (iii) 2.

The design is made of two sub-systems that work as follows:

- The ***3-Bit Asynchronous Counter*** that continuously counts from 0 (Q_2=0, Q_1=0, Q_0=0) to 6 (Q_2=1, Q_1=1, Q_0=0).
- The ***Light Encoder Logic*** that takes the count from the 3-Bit Asynchronous Counter and drives the three output lights **DIV5_6**, **DIV3**, and **DIV2** as follows :
  - The **DIV5_6** output will be on when the count is divisible by 5 or 6.
  - The **DIV3** output will be on when the count is divisible by 3.
  - The **DIV2** output will be on when the count is divisible by 2.

Divisible Detector



Your task is to design the two sub-systems that make up the complete ***Divisible Detector*** that meet the following design specifications.

Design Specifications:

3-Bit Asynchronous Counter

- Must be an ASYNCHRONOUS Counter.
- Must count from 0 to 6.
- Must use J-K flip-flops with Positive Edge Trigger & Active Low SET & RESET.
- May use any additional logic as needed.

Light Encoder Logic

- Must include a K-Map for each output (DIV5_6, DIV3, DIV2) {HINT: The counter never outputs the count 111, thus this should be don't cares in your K-Maps.}
- The logic for the DIV5_6 output may only use 2-Input AND; 2-Input OR; & Logic Inverters (AOI design).
- The logic for the DIV3 output may only use 2-Input NAND gates (NAND only design).
- The logic for the DIV2 output may only use 2-Input NOR gates (NOR only design).

The overall design will be graded based on the following criteria:

- Functionality – Did the design work?
- Specifications – Did you work within the limitations of the design specifications?
- Quality – Did the design use the minimum number of gates/flip-flops required?